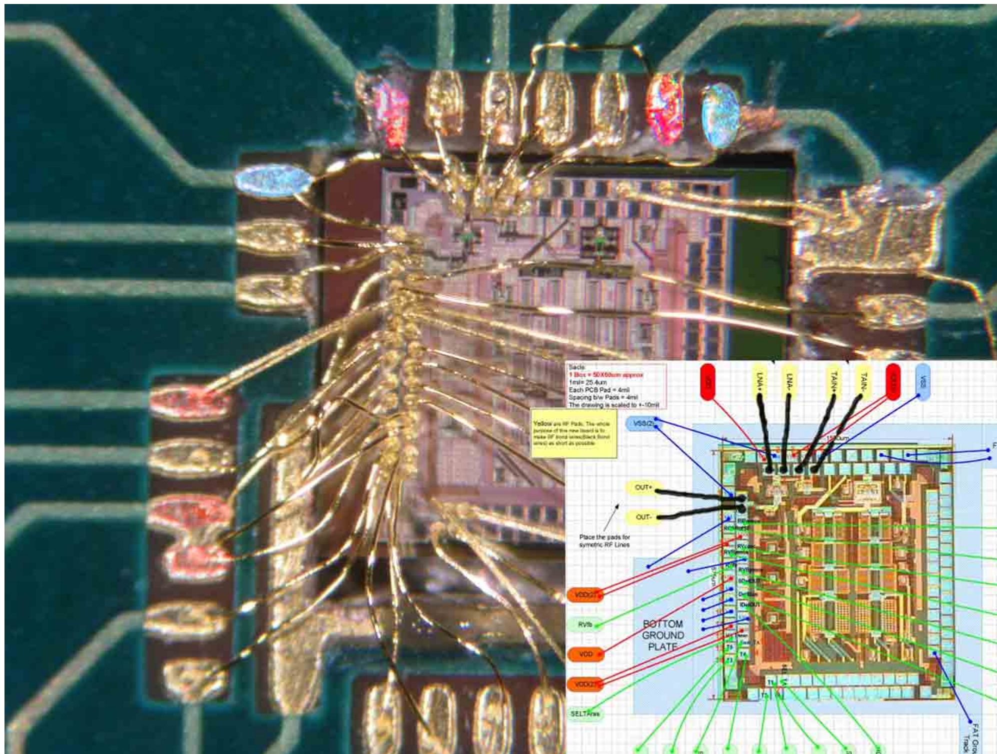
Chip Packaging Design Guide



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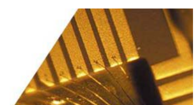

Chip Packaging Design Guide.

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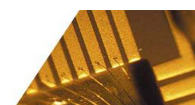


1. Background

Mandalon Technologies AB is a company which provides chip packaging services for prototypes and small series with high demands. In cooperation with the Department of Electrical Engineering ISY at Linköping University a lot of different complex chip prototypes have been handled over the years. The idea of collecting the experience and to form some kind of design guide has been in the minds of some persons for some time.

When minST came into the picture, this was made possible. With minST as one of the financing parts Mandalon and ISY have been able to establish a process and to produce this design guide.

The chips designed at ISY are high performing. The packaging could have an undesired impact on the performance if not considered during the chip design. By using this design guide both increased system performance and reduced time for design, could be achieved.

2. Conclusions

The most obvious conclusion found during the process to produce this design guide, was that there is a need for system thinking early in the design phase.
The chip itself must be integrated successfully on the PCB to function effectively and this PCB-integration must be taken into consideration during the chip design.

3. Introduction

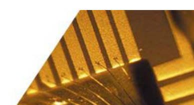
This design guide is based on the experience which Mandalon Technologies has from ball bonding. The equipment, a K&S 4124 is designed for gold bond wires with a diameter between 17-50 µm. The information herein is specific for these circumstances.

The design guide uses three different levels of difficulties (time/cost consuming), with respect to the packaging work. The three different levels shall be considered as an indication.
<u>Time/Cost levels</u>
Level 1: Easy = 1 time/cost unit
Level 2: Normal = 3 time/cost units
Level 3: Close to the Limit = 10 time/cost units

3.1 Document Overview

In chapter 4 *"PCB-Layout - Good to know about PCB-layout before starting to design your chip"* different aspects of the PCB-layout are addressed to help you design a chip suitable for a complete system (including PCB and wire bonding).
Topics such as how to position the pads on the PCB to meet signal requirements and necessary bonding conditions are presented in chapter 4.1-4.3.
Further ways to minimize length of bond wire are presented in chapter 4.4 and 4.5.
Some options on pad-patterns and chip positioning are shown in chapter 4.6 and 4.7.
In chapter 4.8 bonding conditions on the PCB-pads are discussed.

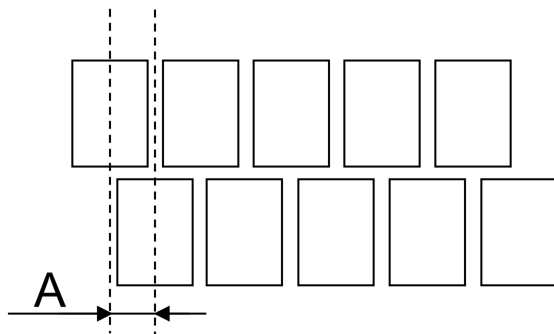
In chapter 5 *"Chip Design - Pitch limitations for bonding"* pitch limitations are addressed to help you design a chip with proper bonding conditions. The special circumstances required for RF signals and data signals are addressed in chapter 5.1 and 5.2 respectively.



3.2 Definitions

In this section you will find some useful definitions.

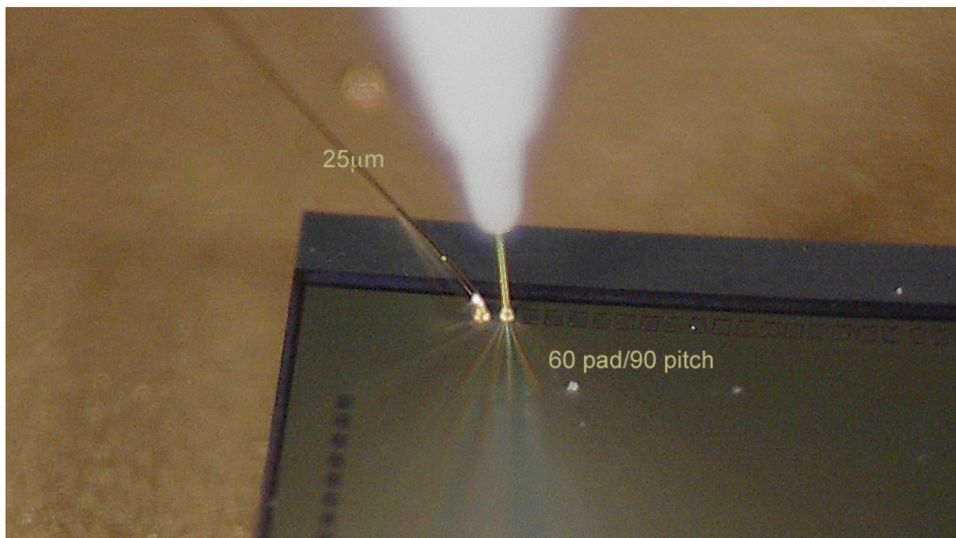
Fan out – Angle spread out of bond wires from the chip to the PCB.
Pitch – The distance in µm between the centres of two subsequent bond-pads on a chip. Also referred to as straight pitch in this document.
Staggered pads – Two rows of pads as in the picture 1 below.
Effective pitch – The distance A in the picture 1 below.



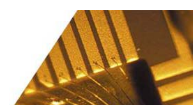
Picture 1. A = effective pitch.

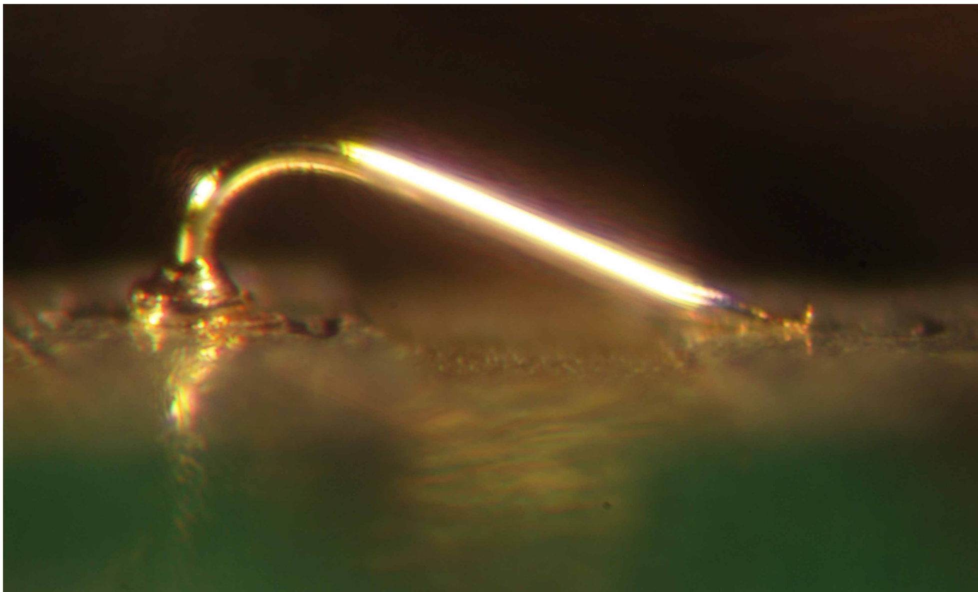
3.3 Ball Bonding

Ball bonding is a bonding method using gold wire. The combination of heat, pressure and ultrasound (US) enables the wire to stick to the bond pads. First a ball is formed at the end of the wire and the ball is then placed on the chip pad and the first bond is performed. The tool is then moved to the PCB pad position, letting out the wire, and the second bond is performed whilst the wire is cut. This becomes a bond without any ball.



Picture 2. Ball bonding with 25 µm wire and pitch 90 µm. A bottleneck capillary is used.





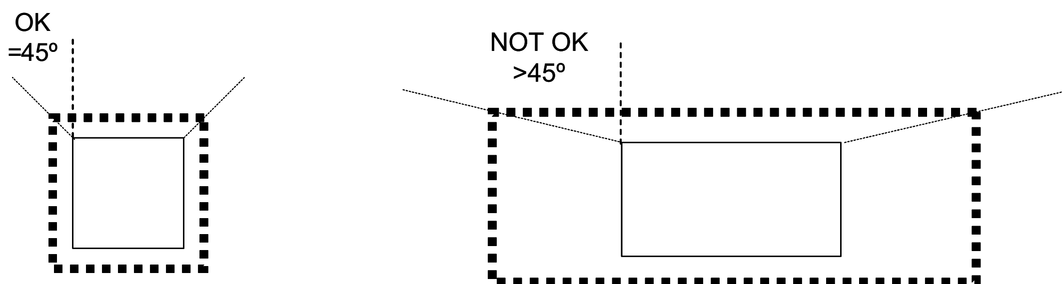
Picture 3. Ball bonding. The difference between 1st bond with the ball and 2nd bond.

4. PCB-Layout - good to know about PCB-layout before starting to design your chip

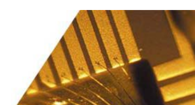
In this chapter different aspects of the PCB-layout are addressed to help you design a chip suitable for a complete packaging system (including PCB and wire bonding).

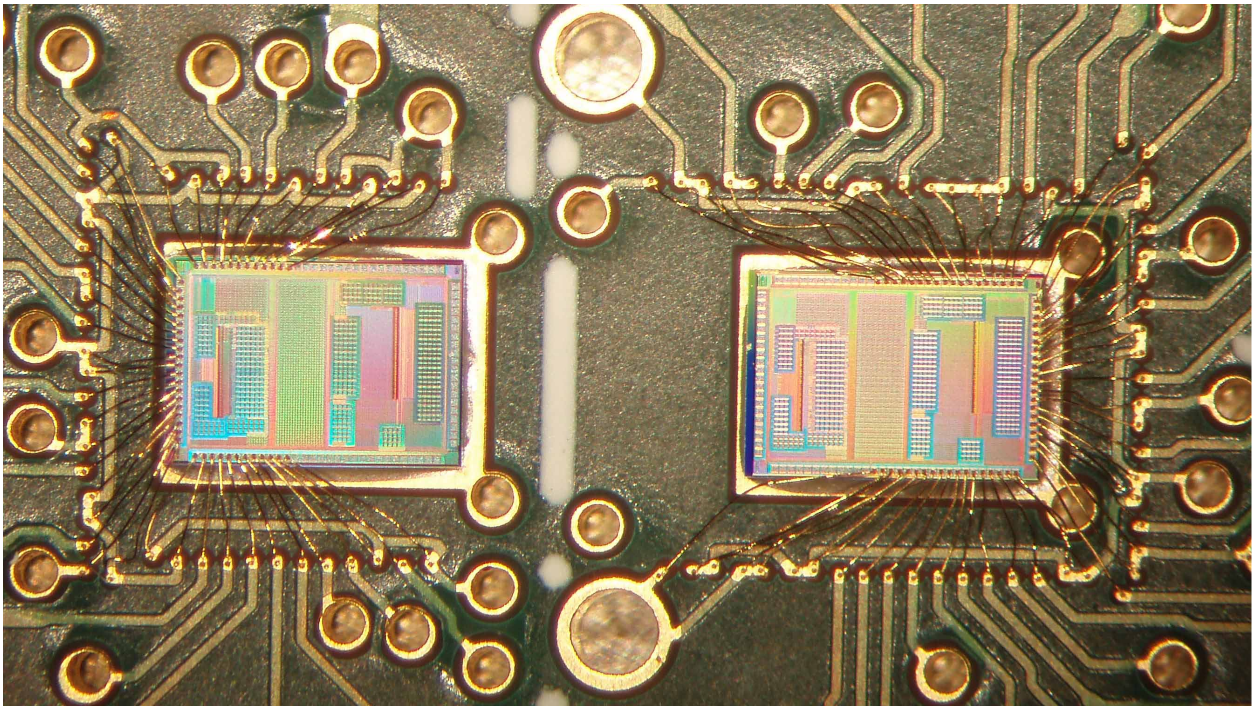
4.1 PCB-Layout – pad positioning to reduce fan out

Angle from chip-pad to PCB-pad above 45º should be avoided. Angles above 45º are likely to cause short circuits between the bond wires.

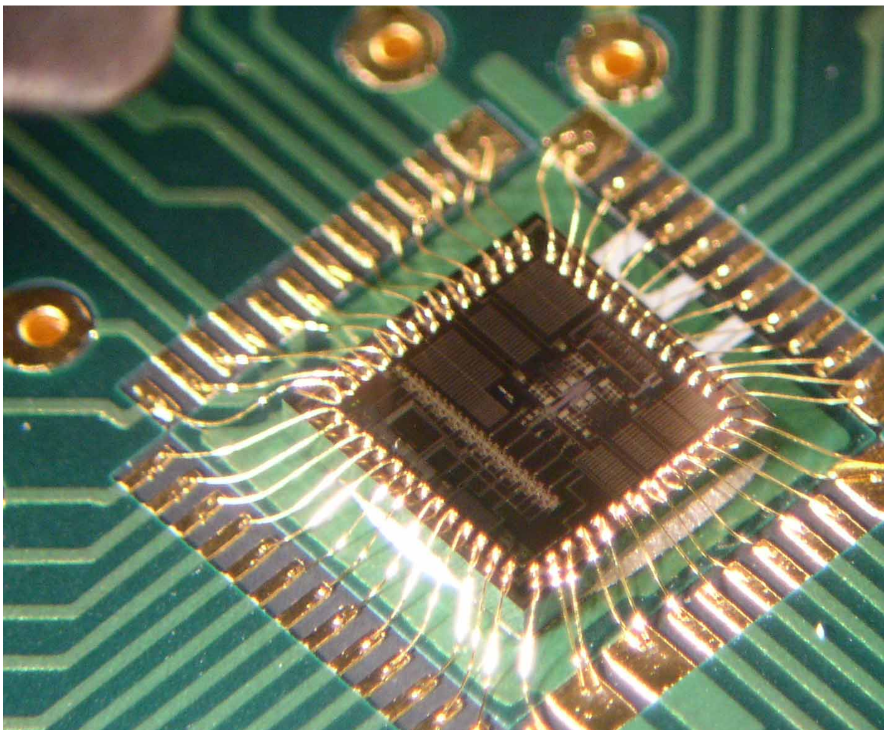


Picture 4. Fan out.

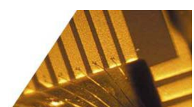


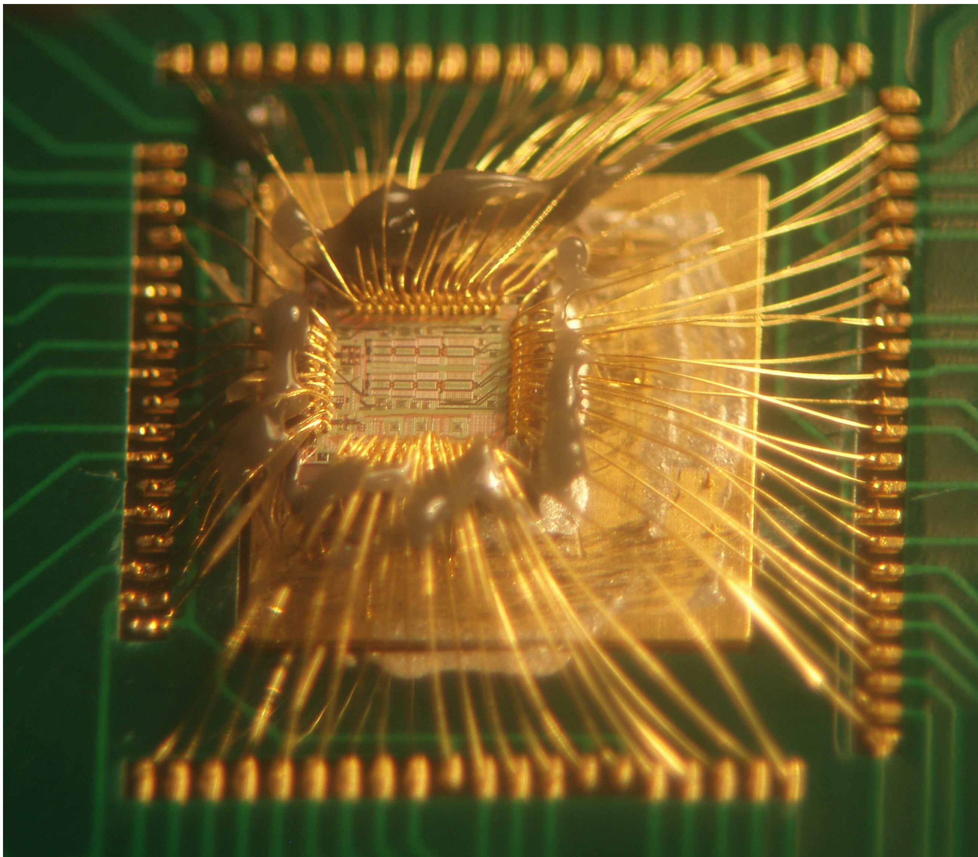


Picture 5. The risk for short circuits increases when angle of fan out is above 45º.

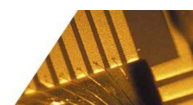


Picture 6. Bonding under normal fan out conditions.



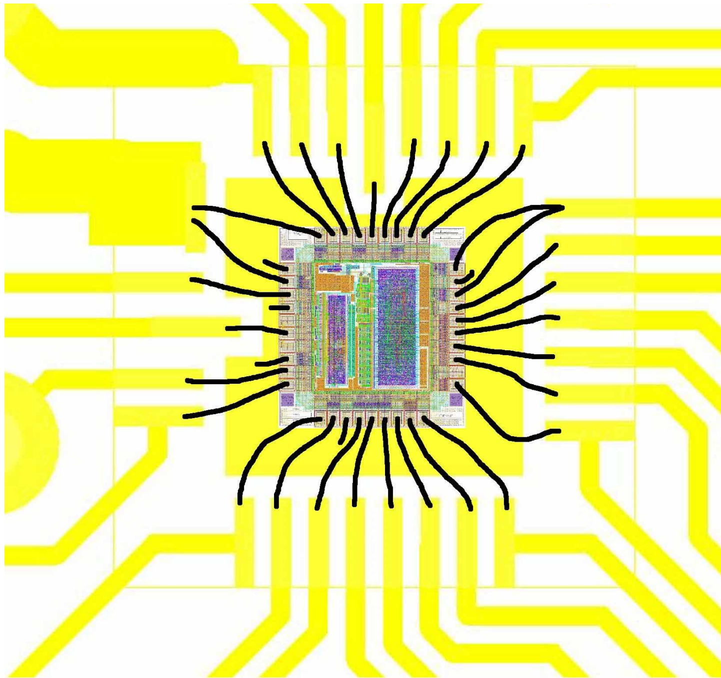


Picture 7. Bonding under difficult fan out conditions. Some fan out >45º. (Cost level 3.)

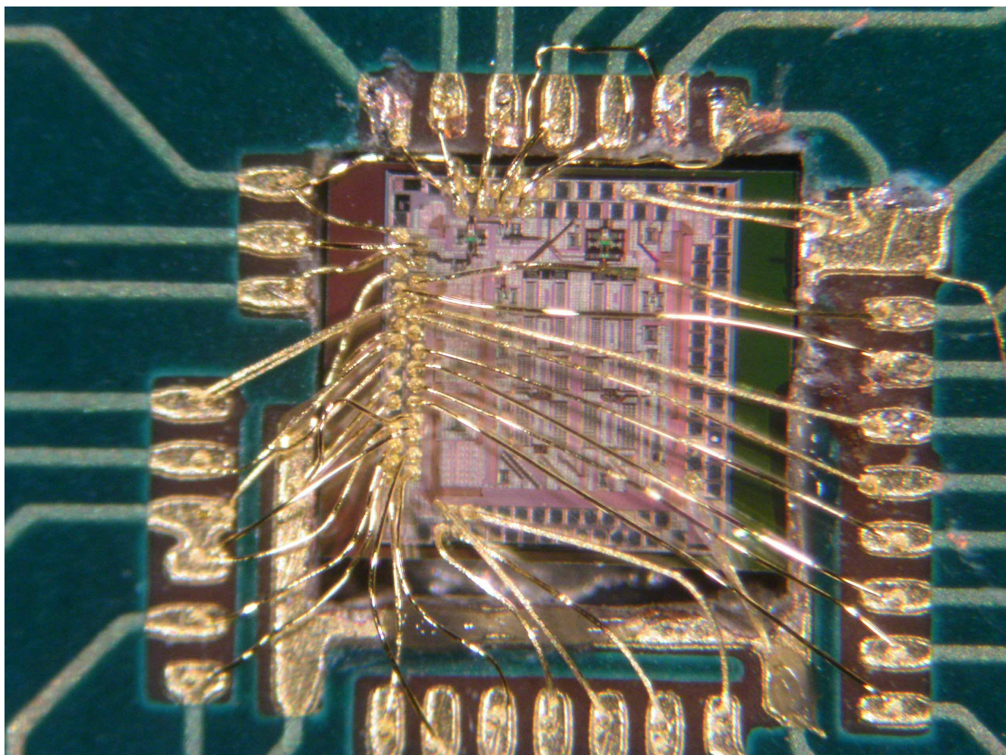


4.2 PCB-Layout - pad positioning (RF signals)

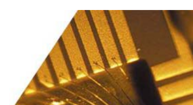
RF signals need shortest possible bond wires between chip and PCB. Start with the signals with the highest requirements. Make sure it is possible to place the pads on the PCB close and with minimum angle.



Picture 8. Note the short bondings in the top middle and left middle.

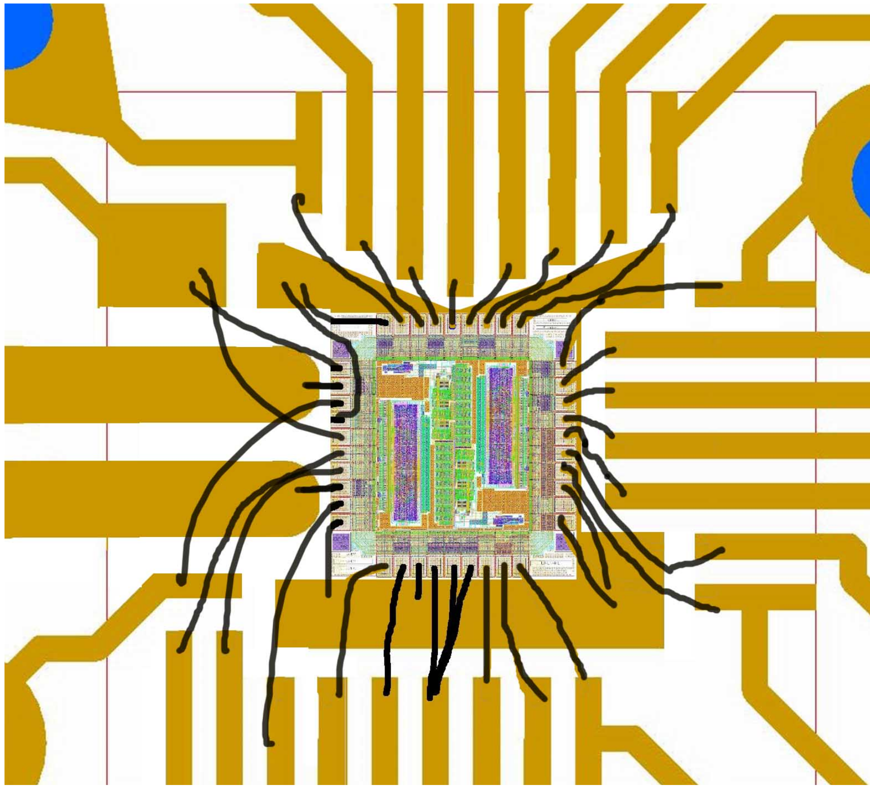


Picture 9. Note the short bondings in the left top corner.

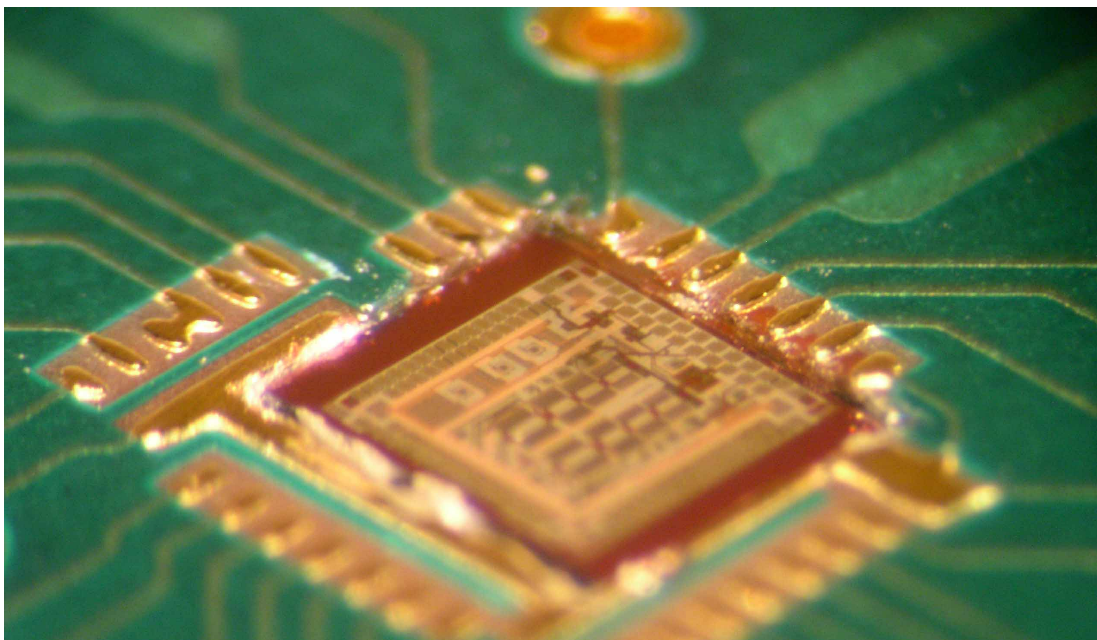


4.3 PCB-Layout - pad positioning (50Ω tracks)

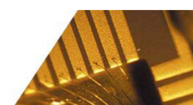
If possible use one side of the PCB for these signals, since there need to be broad tracks/lines on the PCB close to the chip. The bond wires must have minimum length.
The other signals will in this case be wire bonded to the remaining sides of the PCB. This can be good enough for data signals, where long wires are OK.



Picture 10. Example, not a real case.



Picture 11. The broad tracks on the PCB are 50Ω tracks.

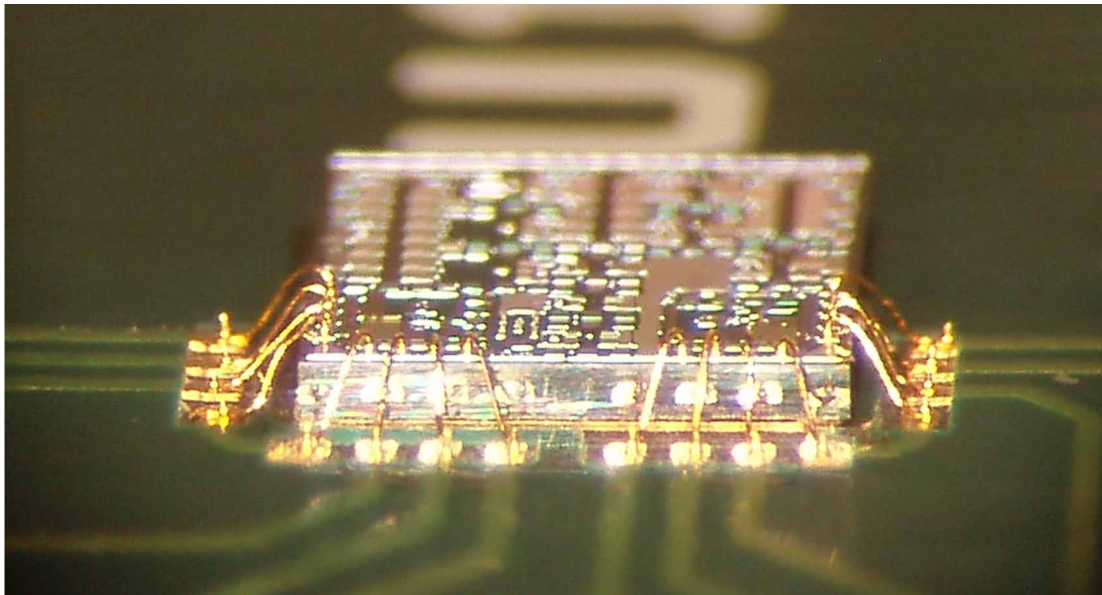


4.4 PCB-Layout - how close to the chip

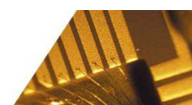
How close to the chip can you bond a wire? It depends on the height on the chip and the angle on the capillary on the bonding equipment. The distances below can be used as an indication.

At chip height ca 500 µm:

Level 1: Easy	>700 µm
Level 2: Normal	500 µm
Level 3: Costly	200 µm



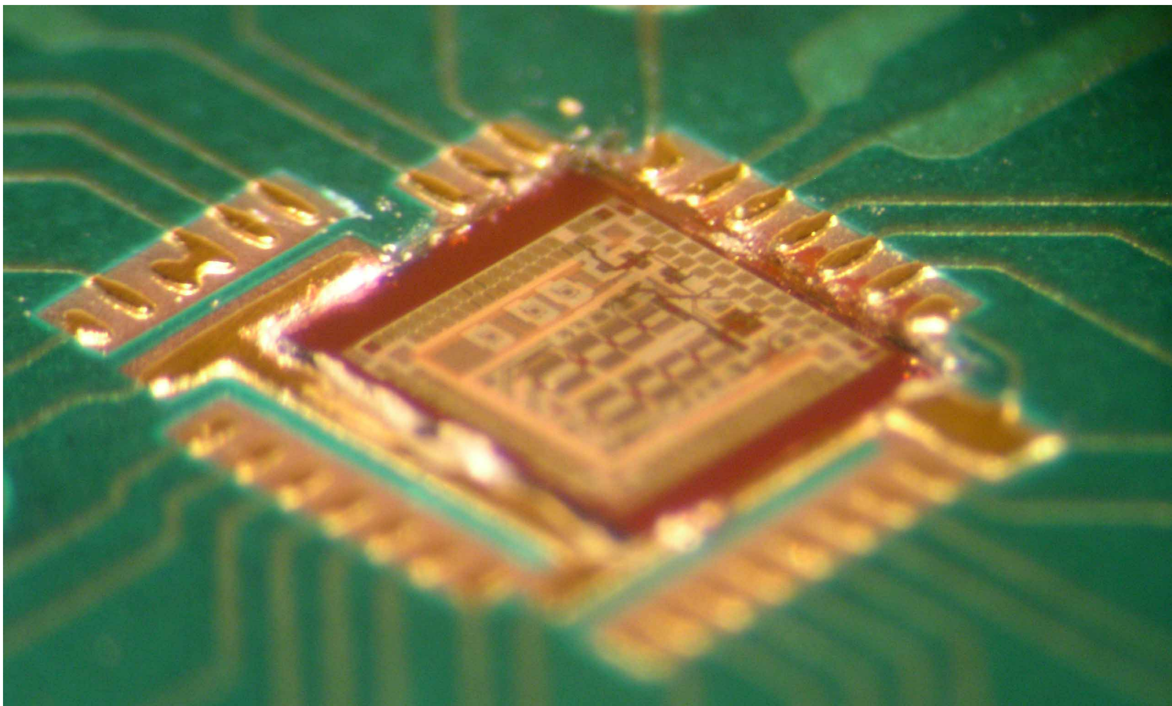
Picture 12. Height of chip is 300 µm. Distance from chip to bond is 250 µm. (Cost level 2-3)



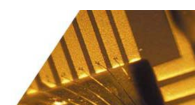
4.5 PCB-Layout – cavity to lower the chip into the PCB

It is possible to prepare a cavity in the PCB where the chip can be placed. This lowers the chip into the PCB, which makes it possible to place the bond wire closer on the PCB.

To be able to make a cavity for the chip, the PCB must be designed for it. There must be only ground layers or no layer at all in the cavity area. If necessary the ground plane may be continued with conducting glue under the chip.
The exact size of the chip must also be known in advance.

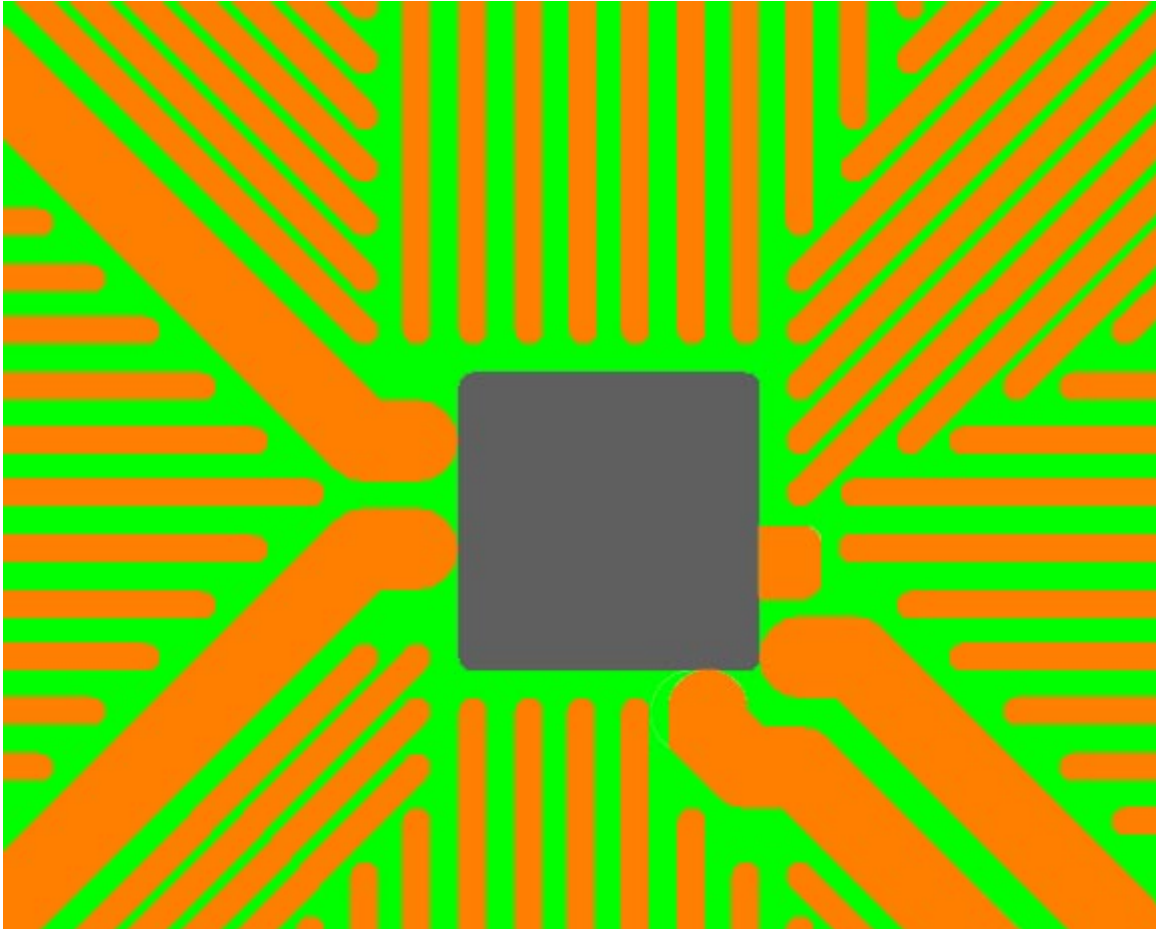


Picture 13. Chip in cavity.



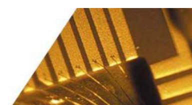
4.6 PCB-Layout – pad patterns

If you have special requirements - don't think symmetry. Here you have some options on PCB-layout for special signals.



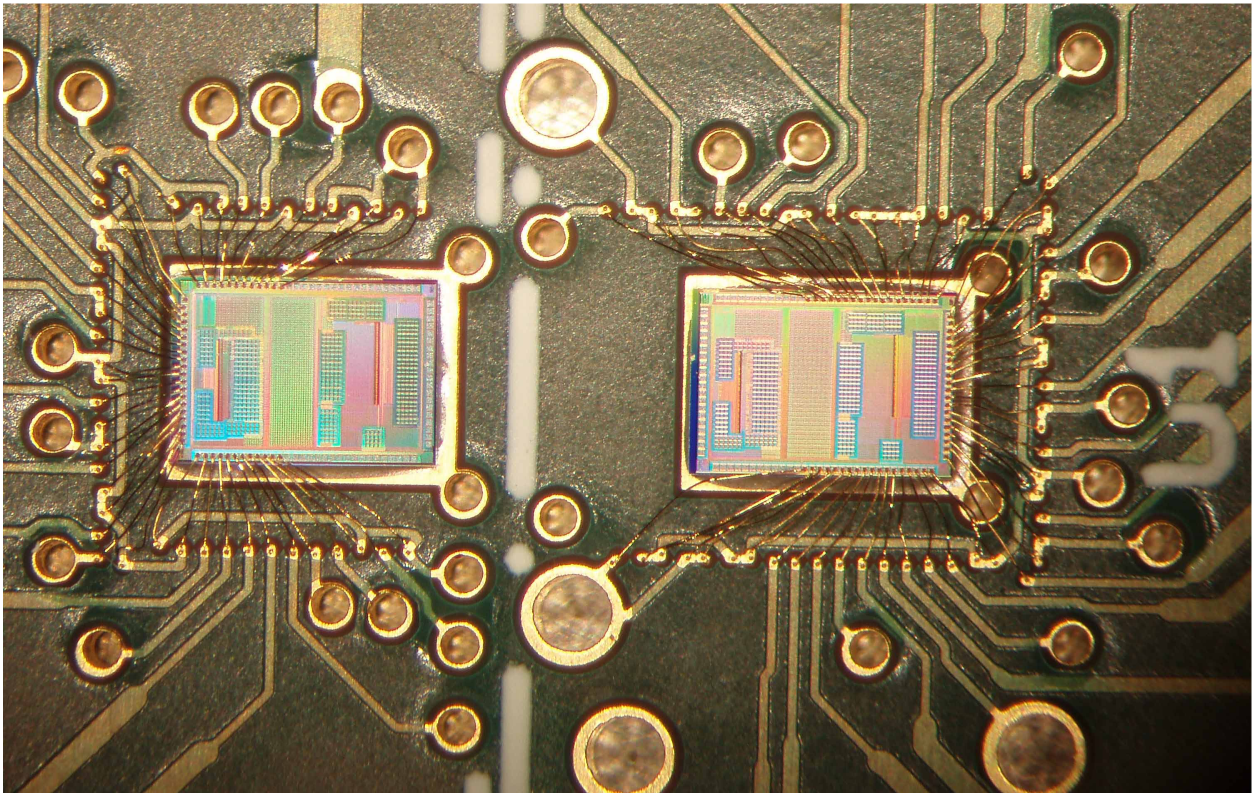
Picture 14. PCB-layout options.

Note that it is possible to bond more than one bond wire to a single pad.



4.7 PCB-Layout – where to place the chip

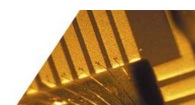
Again if you have special requirements - don’t think symmetry. Here are some options, how to place the chip on the PCB.

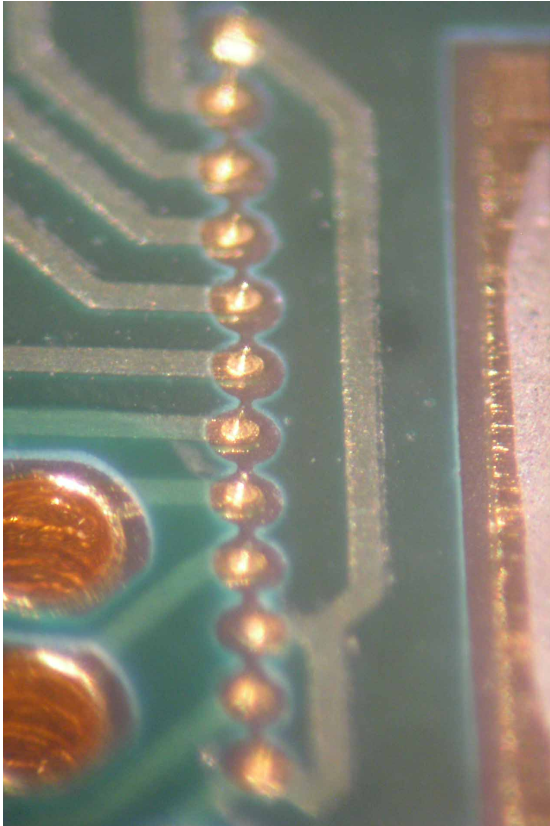


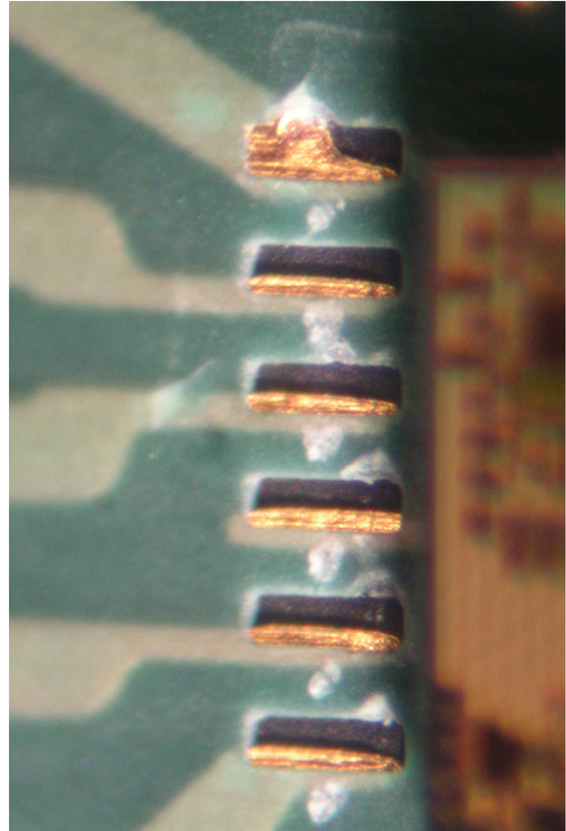
Picture 15. In this case the chip consisted of two separate parts and it was possible to use two chips to avoid further fan out.

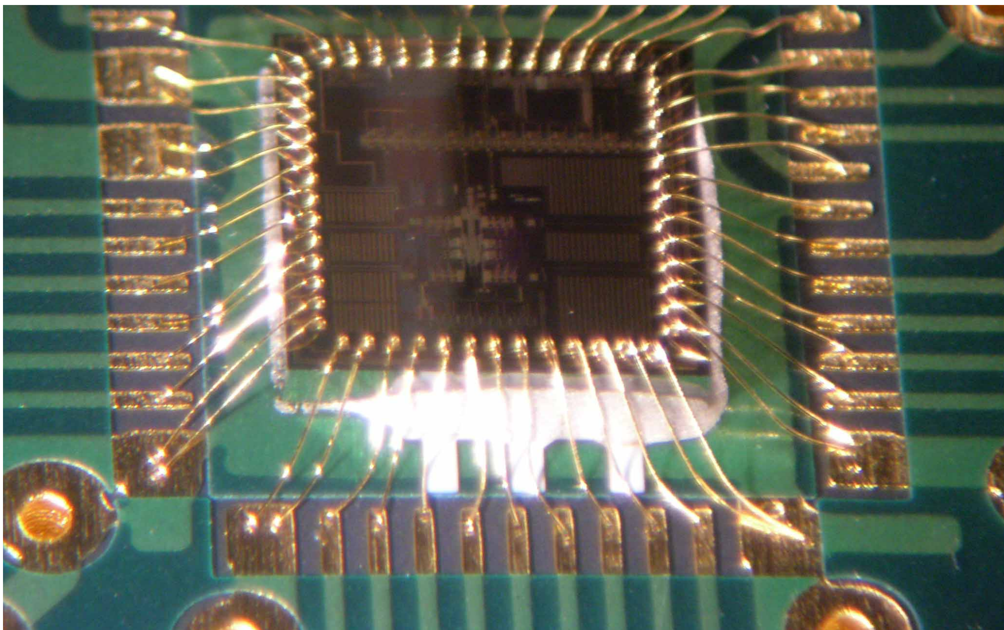
4.8 PCB-Layout - PCB-pad size, open area (longer pads)

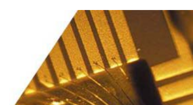
Always consider somewhat longer PCB-pads. If the PCB pads are thin or if the plating for some reason is of poor quality for bonding, longer pads will improve bonding conditions. Also, the possibility of placing the bond a little distance from the very edge provides a more stable bonding surface.




Picture 16. Bond pads bumped in advance. Small open pad area.


Picture 17. Open area do not match pads.


Picture 18. Good bonding conditions with regard to open pad area.



5. Chip Design, Pitch Limitations for Bonding

In this chapter pitch limitations are addressed to help you design a chip with proper bonding conditions for RF signals and for data signals.

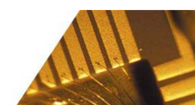
5.1 RF Signals

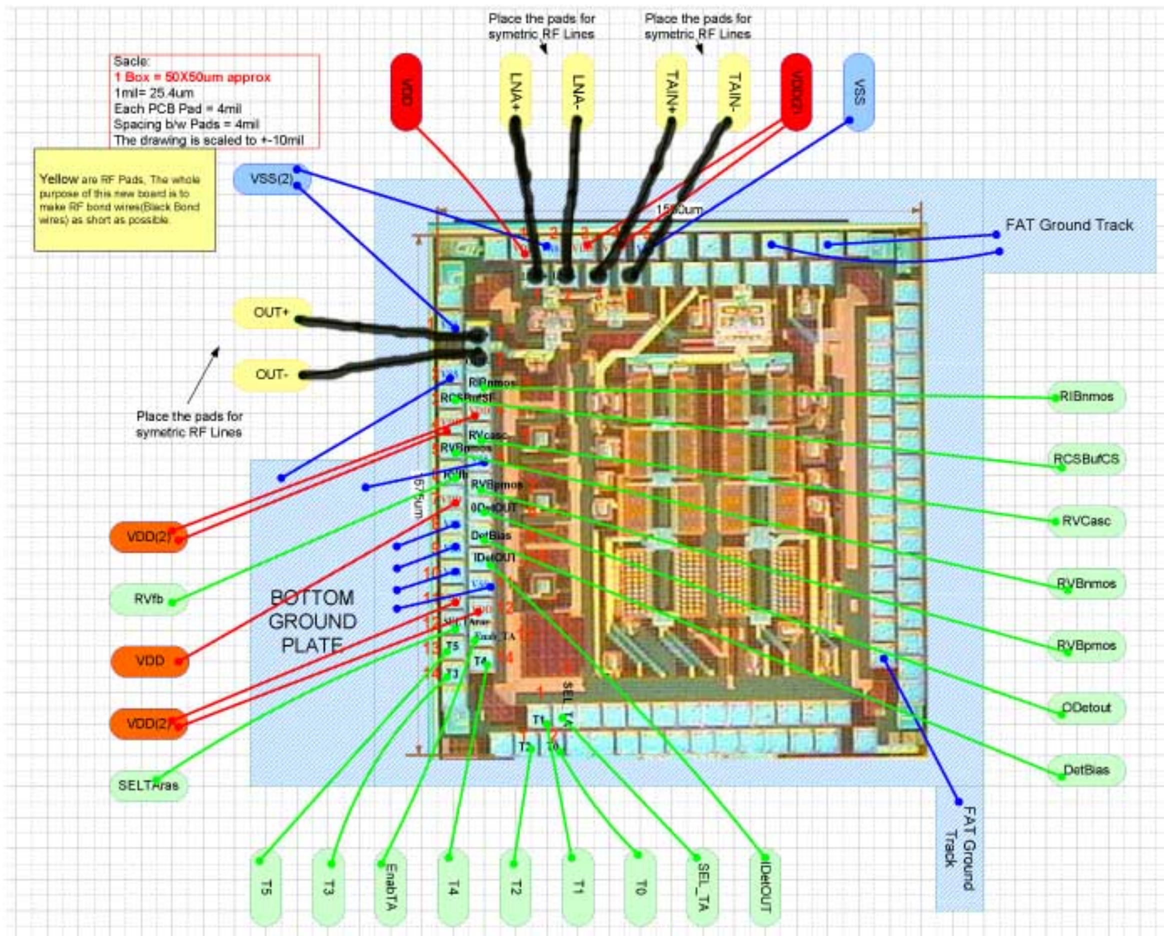
Requirements: short and thick bond wires are required.
Start placing the pads on the chip for the signals with the highest requirements.

There must be enough space for 33µm bond wires for the RF signals.
Example 1:
If you have ca 5 pads with Straight Pitch: Minimum pitch is 100µm.
Example 2:
If you have ca 5 pads with Staggered Pads: Minimum effective pitch is 50µm.

For more examples, see table 1 and table 2 in page 16.

If possible use the outer row on the chip when staggered pads are used as this shortens the bond wire length.
It is of great importance to make sure that the bond wire will be short, by planning for the attachment to the PCB at minimum angle. Also make sure it will not interfere with other bond wires, but can be bonded in a straight line.





Picture 19. Note the thicker 33µm wires and the increased pitch on top row for these specific pads. To the left one pad is left out to provide more space.

Tables

To get an idea of what is possible with regard to pitch and when it starts to get costly, see tables below. One table is for straight pitch and one is for staggered pads.

The tables include three different columns, easy to bond; normal; and close to the limit of what is possible under the stated circumstances. The column to the left shows the smallest pitch, close to the limit of what is possible to perform (with the specific equipment that this design guide is based on) and therefore the most time consuming and expensive.

<u>Time/Cost levels</u>
Level 1: Easy = 1 time/cost unit
Level 2: Normal = 3 time/cost units
Level 3: Close to the Limit = 10 time/cost units

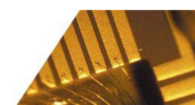


Table 1: Straight Pitch. Case: RF Signals, wire dia = 33µm.

Number of bonds in the specific area	**Level 3: Limit** pitch/wire dia	**Level 2: Normal** pitch/wire dia	**Level 1: Easy** pitch/wire dia
5	100µm /33	125µm /33	150µm /33
10	110µm /33	135µm /33	150µm /33
20	120µm /33	140µm /33	150µm /33

Table 2: Staggered Pads. Case: RF Signals, wire dia = 33µm.

Number of bonds in the specific area	**Level 3: Limit** eff.pitch/wire dia	**Level 2: Normal** eff.pitch/wire dia	**Level 1: Easy** eff.pitch/wire dia
5	50µm /33	60µm /33	75µm /33
10	55µm /33	65µm /33	80µm /33
20	60µm /33	70µm /33	85µm /33

Special cases: Double wires on the same pad are an alternative to thicker wire.

5.2 Data Signals

Requirements: Small pitch is required to minimize chip area used for pads.

The following apply for data signals that can have long bond wires and where there are no specific requirements on the wire diameter.

Smallest possible pitch is decided by the wire diameter. A rule of thumb is that the pitch must be at least 2,5 * the wire diameter, as the ball formed will be of that size.

Smaller pitch increase time and therefore the cost for bonding. An increased number of bonds add another practical limit, since one single not perfectly placed bond will interfere with all the following bonds in that row. This is why all bonds on the chip should be included, when reading column 1 “Number of bonds on the chip”, in table 3 and 4 below.

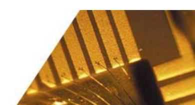
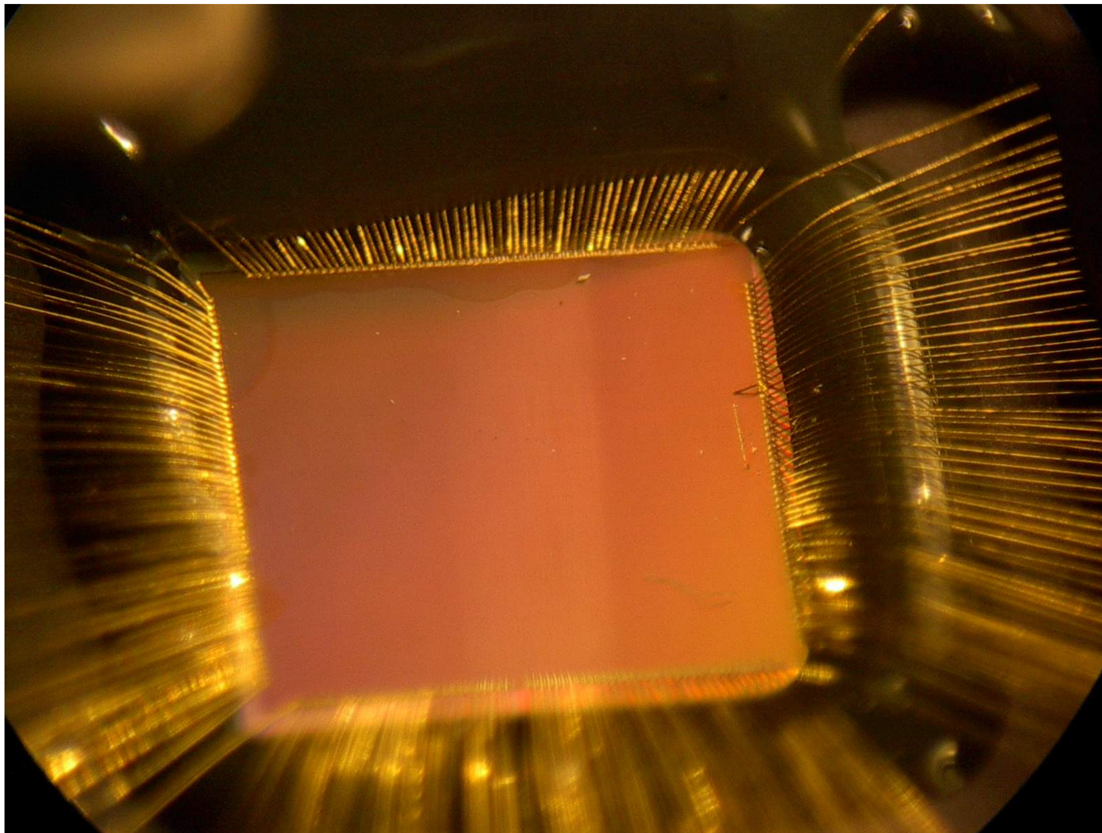


Table 3: Straight pitch. Case: Data Signals.

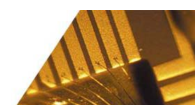
Number of bonds on the chip	Level 3: Limit pitch	/wire dia	Level 2: Normal pitch	/wire dia	Level 1: Easy pitch	/wire dia
2	45-50µm	/17	60µm	/17	80µm	/25
5	50-55µm	/17	65µm	/17		
10			70µm	/20		
20	55-60µm	/17	80-90µm	/25	100µm	/25
50			90-95µm	/25		
100			95-100µm	/25		
200	60µm	/17	100µm	/25	150µm	/33

Choose the smallest pad size if there are more than 20 wires and if the pitch is 65µm or below. In these cases the conditions for bonding are tight and the risk of a bond ball causing short circuit between pads needs to be reduced.

Note:
The thinnest bond wire, 17µm, always makes the bonding procedure more sensitive. This increases time for bonding and therefore the cost.
To be able to bond 70µm or smaller pitch, the 17µm bond wire is normally required.



Picture 20. Bonding with 17µm wire and 60 pitch. (Cost level 3.)



Staggered pads

If the number of wires are high use staggered pads on the chip. Note that this requires special attention to the PCB-layout, to avoid fan out >45º.

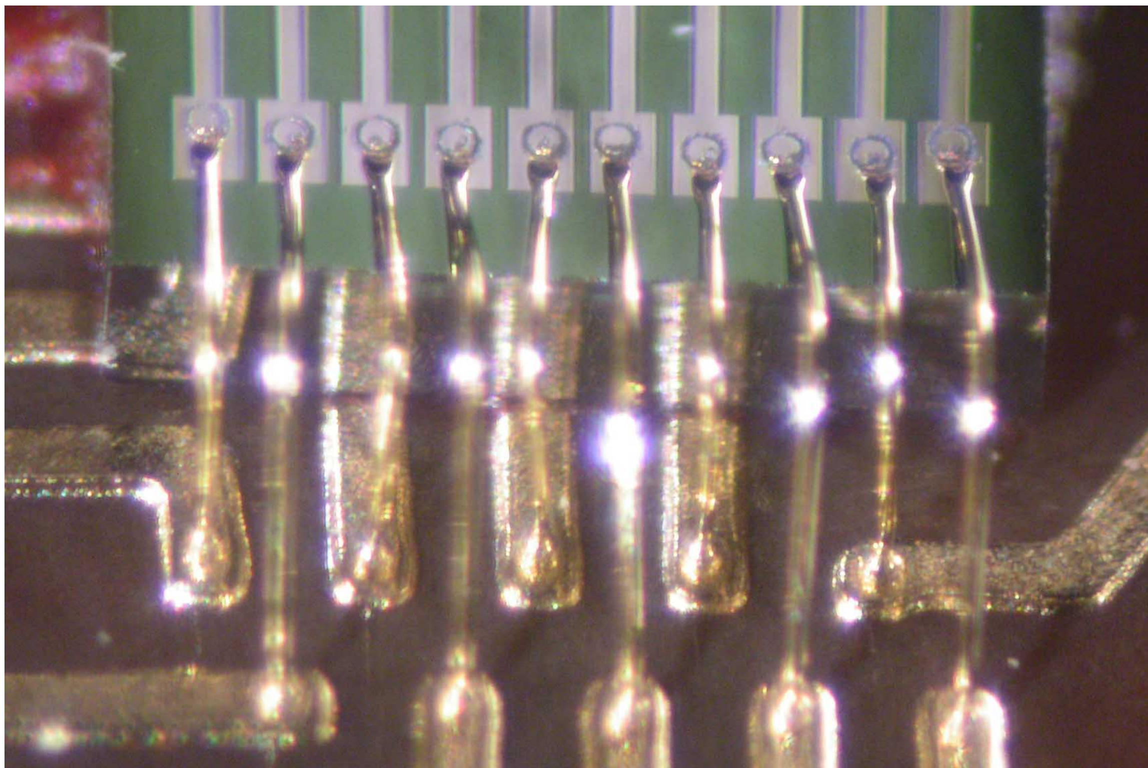
When smallest pitch is used and the number of bond wires is very high, if the library allows a bigger distance (30-40 µm instead of 10 µm) between the two rows of pads in staggered pads, use a bigger distance to improve bonding conditions.

Table 4: Staggered pads. Case: Data Signals.

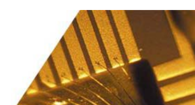
Number of bonds on the chip	**Level 3: Limit** eff.pitch/wire dia	**Level 2: Normal** eff.pitch/wire dia	**Level 1: Easy** eff.pitch/wire dia
10	30µm /17	40µm /25	
20	35µm /17	45µm /25	55µm /25
50	40µm /17	50µm /25	60µm /25

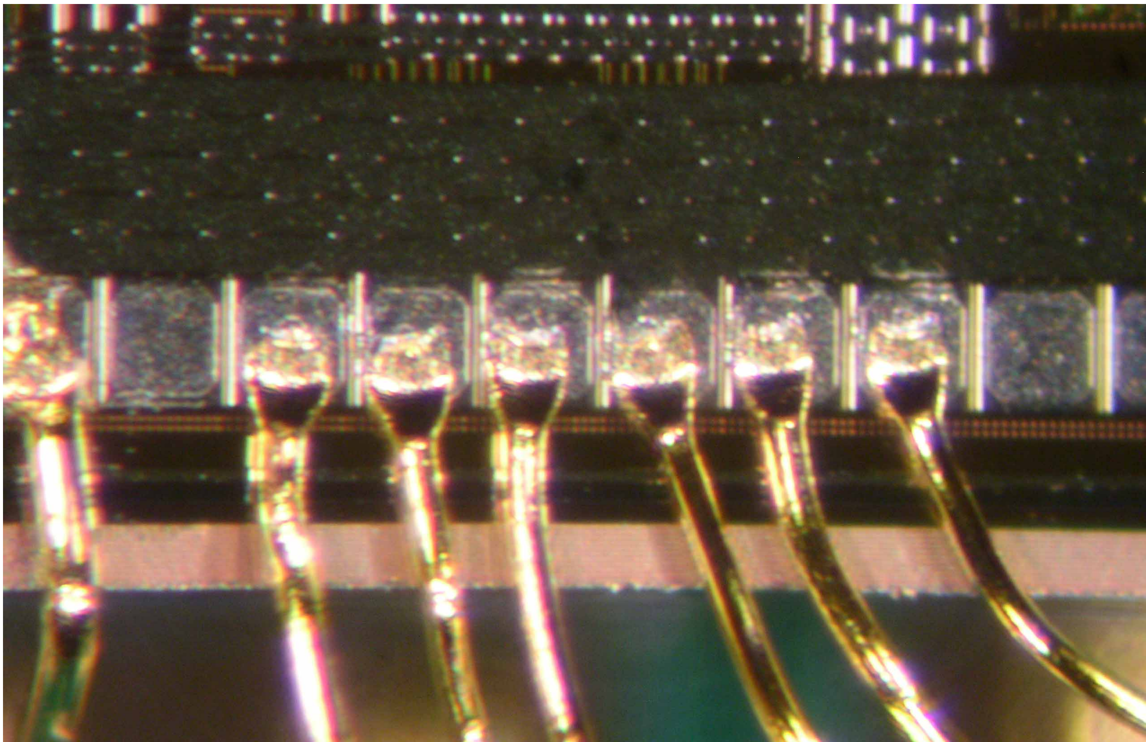
Special cases:

- Reverse bonding (first bond with the ball on the PCB) could be used to reduce space needed on the chip, but it requires a robust surface around the chip-pad.



Picture 21. Reverse bonding with marks on the chip at the second bond.





Picture 22. Reverse bonding, no marks at the second bond.

6. System thinking

To be able to get the most out of a chip the total system must perform as well as the chip itself. The integration of chip and PCB is a critical part of the design.

Consider the PCB-layout already during the chip design phase, (see chapter 4 of this design guide) and involve the packaging partner early.

Another tool that could be of assistance is to produce a layout drawing. This helps all people involved to understand the special demands of the system. See picture 8 for example.